L Number	Hits	Search Text	DB	Time stamp
1	149	(438/350).CCLS.	USPAT; US-PGPUB	2002/07/31 17:09
2	1554	"internal base" or "external base"	USPAT; US-PGPUB	2002/07/31 17:10
4	54052	438/$.ccls.	USPAT; US-PGPUB	2002/07/31 18:18
5	204	("internal base" or "external base") and 438/$.ccls.	USPAT; US-PGPUB	2002/07/31 17:10
3	13	((438/350).CCLS.) and ("internal base" or "external base")	USPAT; US-PGPUB	2002/07/31 17:25
6	246	buie	USPAT; US-PGPUB	2002/07/31 17:25
7	49683	triple	USPAT; US-PGPUB	2002/07/31 17:25
8	10	buie and triple	USPAT; US-PGPUB	2002/07/31 17:26
9	143526	internal with external	USPAT; US-PGPUB	2002/07/31 18:18
10	54002	bipolar	USPAT; US-PGPUB	2002/07/31 18:19
11	3939	(internal with external) and bipolar	USPAT; US-PGPUB	2002/07/31 18:19
12	4260	(internal with external) with base	USPAT; US-PGPUB	2002/07/31 18:19
13	164	((internal with external) and bipolar) and ((internal with external) with base)	USPAT; US-PGPUB	2002/07/31 18:19
14	315948	@ad>19990812 or @rlad>19990812	USPAT; US-PGPUB	2002/07/31 18:20
15	150	(((internal with external) and bipolar) and ((internal with external) with base)) not (@ad>19990812 or @rlad>19990812)	USPAT; US-PGPUB	2002/07/31 18:21
16	515738	concentration	USPAT; US-PGPUB	2002/07/31 18:21
17	25	concentration with ((internal with external) with base)	USPAT; US-PGPUB	2002/07/31 18:21
18	24	(concentration with ((internal with external) with base)) not (@ad>19990812 or @rlad>19990812)	USPAT; US-PGPUB	2002/07/31 18:22

external/internal
intrinsic/extrinsic
base (with) surround & quitter

L Number	Hits	Search Text	DB	Time stamp
1	149	(438/350).CCLS.	USPAT; US-PGPUB	2002/07/31 17:09
2	1554	"internal base" or "external base"	USPAT; US-PGPUB	2002/07/31 17:10
4	54052	438/$.ccls.	USPAT; US-PGPUB	2002/07/31 17:10
5	204	("internal base" or "external base") and 438/$.ccls.	USPAT; US-PGPUB	2002/07/31 17:10
3	13	((438/350).CCLS.) and ("internal base" or "external base")	USPAT; US-PGPUB	2002/07/31 17:25
6	246	buie	USPAT; US-PGPUB	2002/07/31 17:25
7	49683	triple	USPAT; US-PGPUB	2002/07/31 17:25
8	10	buie and triple	USPAT; US-PGPUB	2002/07/31 17:26

FIG. 2

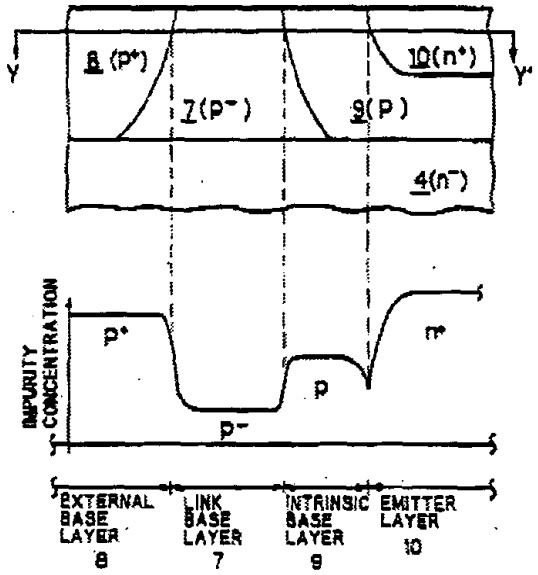


Fig. 3 PRIOR ART

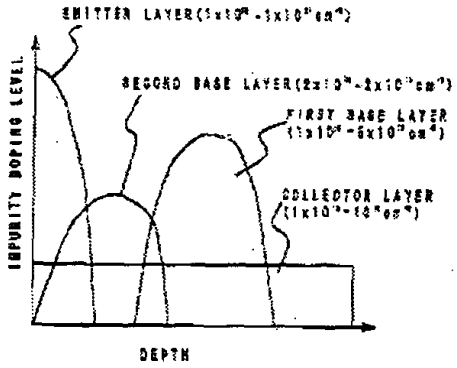
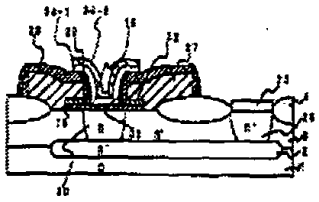


Fig. 16



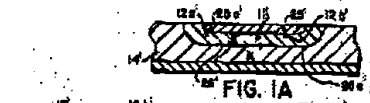


FIG. 1A

FIG. 3A

FIG. 4A

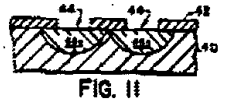


FIG. 11

FIG. 12

FIG. 13

FIG. 14

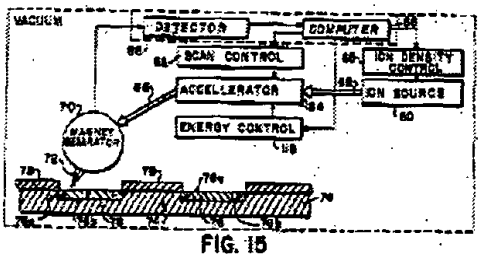


FIG. 15

INVENTOR
EDWARD SIMON
BY
ATTORNEYS

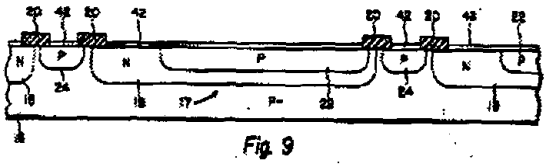


Fig. 9

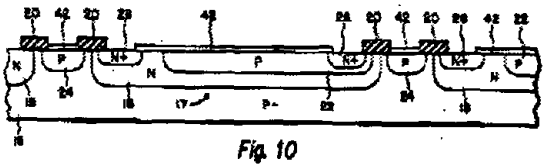


Fig. 10

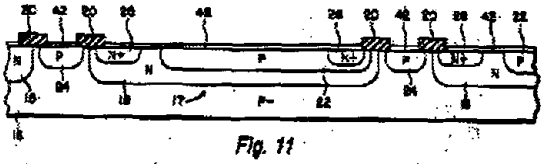


Fig. 11

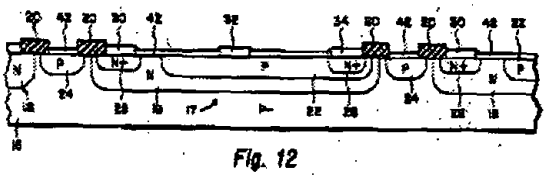


Fig. 12

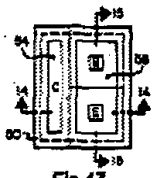


Fig. 13


Fig. 14


Fig. 15

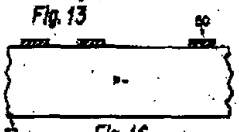


Fig. 16

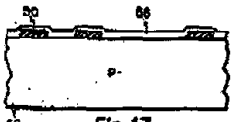


Fig. 17

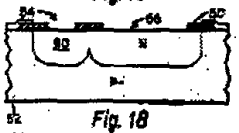


Fig. 18

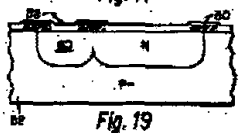


Fig. 19

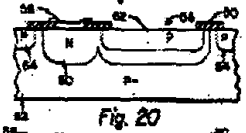


Fig. 20

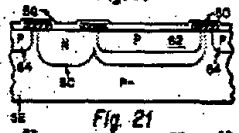


Fig. 21

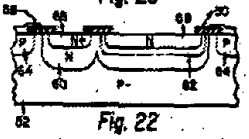


Fig. 22

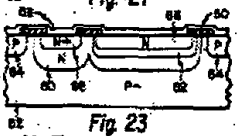


Fig. 23

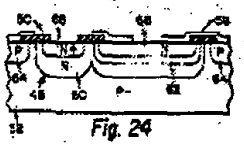


Fig. 24

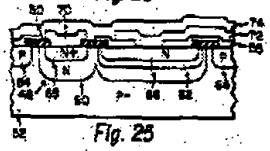


Fig. 25

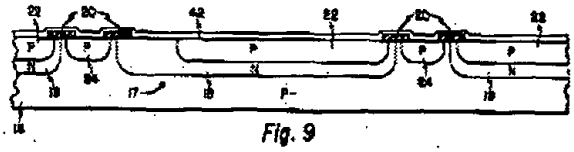


Fig. 9

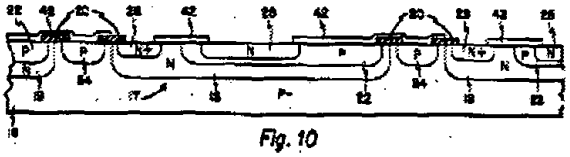


Fig. 10

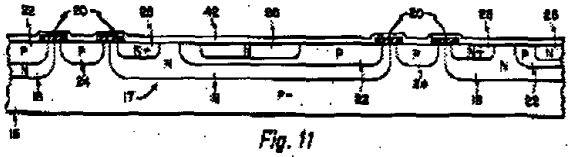


Fig. 11

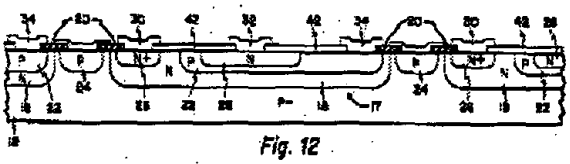


Fig. 12

EAST Browser - L8: (10) 6 and 7 | US 4111720 | Tag: 5 | Doc: 6/10 (SORTED) | "Full" 1/7 (Total images 7)

File Edit View Tools Window Help

United States Patent [19]

Michel et al.

[11] **4,111,720**

[45] **Sep. 5, 1978**

[54] METHOD FOR FORMING A NON-EPITAXIAL BIPOLAR INTEGRATED CIRCUIT

[75] Inventors: Alvin E. Michel, Ossining; Robert O. Schwenker, Hopewell Junction; James F. Ziegler, Putnam Valley, all of N.Y.

[73] Assignee: International Business Machines Corporation, Armonk, N.Y.

[21] Appl. No.: [illegible]

[22] Filed: Mar. 21, 1977

[51] Int. Cl.[2] .... [illegible]

[52] U.S. Cl. .... [illegible]

[58] Field of Search .... [illegible]

[56] References Cited

U.S. PATENT DOCUMENTS

[illegible]	[illegible]	McCaldin	[illegible]
[illegible]	[illegible]	Lepselter	[illegible]
[illegible]	[illegible]	Li	[illegible]
[illegible]	[illegible]	Watanabe et al.	[illegible]
[illegible]	[illegible]	Duffy et al.	[illegible]
[illegible]	[illegible]	[illegible] et al.	[illegible]
[illegible]	[illegible]	Evans et al.	[illegible]
[illegible]	[illegible]	Abbas et al.	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible] et al.	[illegible]
[illegible]	[illegible]	[illegible] et al.	[illegible]

OTHER PUBLICATIONS

Ziegler et al., "Self-Isolating Buried Collector . . . Transistor", IBM Tech. Bul. Disc. 14, (1972) [illegible].

P. W. Martin "Integrated [illegible] . . . Detectors . . . by Ion Implantation", Nucl. Instr. and Methods [illegible] (1969) [illegible].

[illegible] et al., "Preventing Inversion . . . Large Scale . . . Devices" IBM Tech. Discl. Bull. 17 (1975) [illegible].

J. [illegible], "Improved Triple Diffusion Means Denser LOCFET" Electronics, Aug. 1975, [illegible].

Ziegler et al., ". . . High Energy Ion Implantation . . . for Pedestal Collectors," IBM Jr. of R & D, 15 (1971), [illegible].

Primary Examiner—[illegible] Dean

Assistant Examiner—Upendra Roy

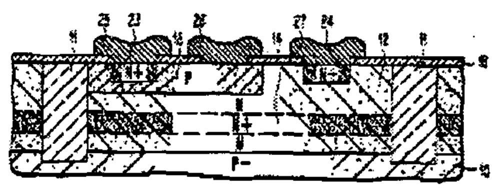
Attorney, Agent, or Firm—J. B. Kraft

[57] ABSTRACT

A method for forming a non-epitaxial bipolar integrated circuit comprising first forming in a silicon substrate of one-type of conductivity, recessed silicon dioxide regions extending into the substrate and laterally enclosing at least one silicon substrate region of said one-type conductivity. Then, forming by ion implantation the first region of opposite-type conductivity which is fully enclosed laterally by said recessed silicon dioxide. This region is formed by directing a beam of ions of opposite-type conductivity impurity at said enclosed silicon region at such energy and dosage levels that the opposite conductivity-type impurity introduced into the substrate in said region will have a concentration peak at a point below the surface of this first region. Then, a region of said one-type conductivity is formed which extends from the surface into said first opposite-type conductivity region to a point between said concentration peak and said surface. Next, a second region of said opposite-type conductivity is formed which extends from the surface part way into said region of one-type conductivity.

Preferably, the ion beam energy level is at least one MeV, and said concentration peak is at least one micron below the surface. It is further preferable that the energy and dosage levels of the beam of ions are selected so that the opposite-type conductivity impurity has a more gradual distribution gradient between the peak and the surface than between the peak and the junction of the first region with the substrate.

13 Claims, 4 Drawing Figures



Details Text Image HTML Full

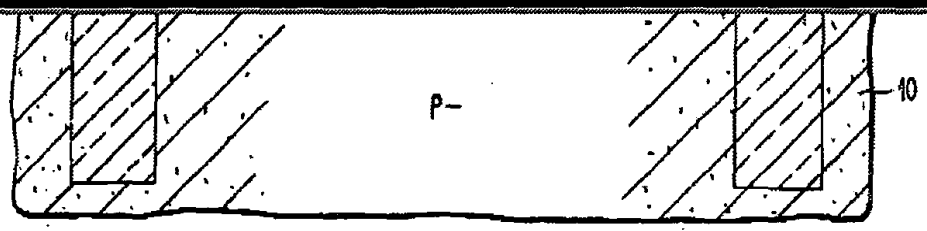


FIG. 1A

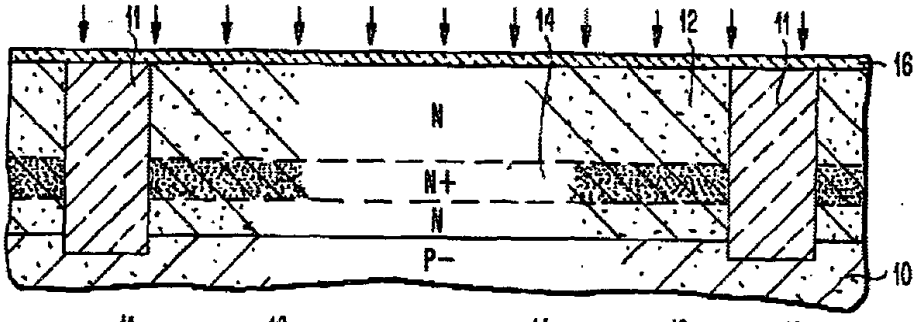


FIG. 1B

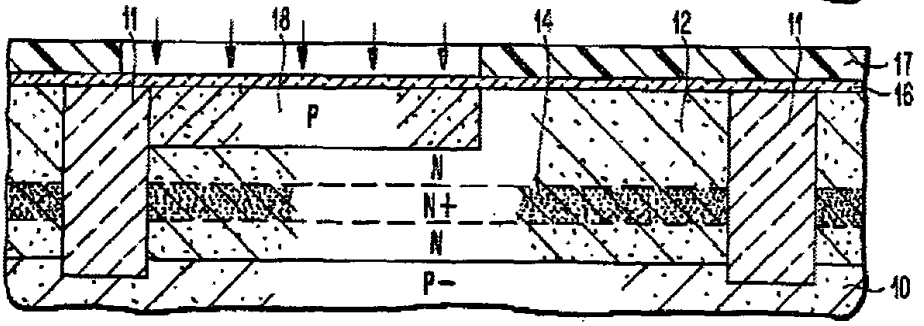
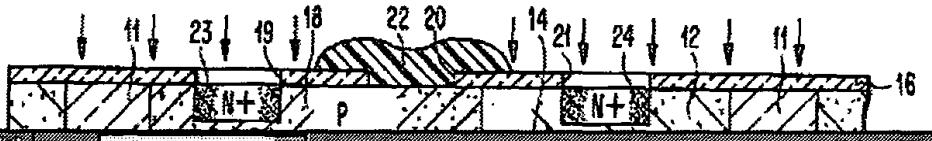


FIG. 1C



US-PAT-NO: 5986327

DOCUMENT-IDENTIFIER: US 5986327 A

TITLE: Bipolar type diode

---------- KWIC ---------

In the diode shown in FIG. 7, an emitter region 5 and base region 4 are formed over a silicon semiconductor substrate 1, the concentrations of the emitter and base regions having the same level as those in FIG. 1 but, here, an internal base region 16 and external base region 17 are formed over the substrate, an aspect which is different from that shown in FIG. 1. Further, a phosphorus (P) of about 10.sup.20 /cm.sup.3 is diffused to provide a collector contact 18. The internal base region 16 has a junction depth Xj of 0.5 to 0.6 .mu.m and concentration of 10.sup.17 /cm.sup.3 and the external base region 17 has a junction depth Xj of 0.7 to 0.8 .mu.m and concentration of 10.sup.18 /cm.sup.3.

FIG. 14 is a cross-sectional view showing a major section of a bipolar IC device incorporating the aforementioned zener diode therein. Island areas are formed in an N type epitaxial layer 30a of a P type polysilicon semiconductor substrate 30 in a manner to be isolated by P type isolation areas 31. An NPN

Subsequently, as shown in FIG. 8(b), an opening 106a is bored on the upper portion over the N.sup.+ -type buried region 102 out of the oxide film 106. Through this opening 106a .sup.11 B ions (designated by Reference Numeral 107) are implanted to form a P.sup.- -type (a low impurity concentration P-type) active base 108. Then as shown in FIG. 8(c), on the surface of the substrate, a resist 110 is applied, followed by performing photolithography to bore an opening 110a in a region corresponding to the periphery of the active base 108 out of the resist 110. Through this opening 110a .sup.11 B ions are implanted to form a P.sup.+ -type (a high impurity concentration P-type) external base 111 on the periphery of the active base 108 (incidentally out of the active base 108 a portion where P.sup.- type remains is referred to as an "internal base"). After removing the resist 110, as shown in FIG. 9(a), an oxide film 112 is formed on the opening 106a. Then as shown in FIG. 9(b), on a portion corresponding to a portion above the internal base 108a an opening 112a is bored followed by ion implanting As ions to form an N.sup.+ -type emitter region 114 on the surface of the internal base 108a. After this step, as shown in FIG. 9(c), an oxide film 115 is provided on the entire surface. With a known method a collector electrode 116, a base electrode 117 and an emitter electrode 118 are then formed.

This vertical NPN transistor can have a favorable ohmic contact with the base electrode 117 on the high impurity concentration (p.sup.+) external base 111 while controlling the current amplification rate hFE at the low concentration (n.sup.-) internal base 108a.

US-PAT-NO: 5523242

DOCUMENT-IDENTIFIER: US 5523242 A

TITLE: Method of manufacturing a BiMOS device

--------- KWIC ---------

The external base region of the bipolar transistor has an intermediate concentration value between the concentrations of the external base electrode and an internal base region.

US-PAT-NO: 5512772

DOCUMENT-IDENTIFIER: US 5512772 A

TITLE: Semiconductor device having bipolar transistor and MOS transistor

--------- KWIC --------

Next, as shown in FIG. 5C, mixed crystal of silicon and germanium is formed and then a heat treatment (at 600.degree. to 900.degree. C.) is effected in order to crystallize the silicon. As a result, an internal base region (mixed crystal of silicon and germanium) 95a containing a P.sup.- -type impurity and an external base region 95b containing a P.sup.+ -type impurity and having an impurity concentration higher than the internal base region 95a are formed in the amorphous silicon layer 93. Further, arsenic is ion-implanted into the surface area of the amorphous silicon layer 94 at a high impurity concentration to form an N.sup.+ -type region. Next, the amorphous silicon layer 94 is patterned to form an emitter region. After this, a SiGe layer formed of the internal base region 95a and the external base region 95b is selectively etched to lie over the field oxide film 85 so as to form a base region. Next, an inter-level insulation film 96 is deposited on the entire surface by use of the CVD method, and then a heat treatment is effected at 1000.degree. C. for approx. 10 seconds. Contact holes reaching the base region and the like are

US-PAT-NO: 5409848

DOCUMENT-IDENTIFIER: US 5409848 A

TITLE: Angled lateral pocket implants on p-type semiconductor devices

---------- KWIC ---------

U.S. Pat. No. 5,100,810 relates to a method of simultaneously manufacturing n-p-n BIP elements and MOS field-effect transistors (MOSFETs). In particular, a semiconductor layer composed of a semiconductor layer of one conductivity type on which a high-concentration semiconductor layer of the same type is formed on the surface of a insulating substrate. By selectively etching the semiconductor layer, the high-concentration external base region of the first conductivity type is left, and at the same time, only a thicker prospective internal base region just under the external base region and a prospective emitter region and prospective collector region, which are located at both sides of the prospective internal base region and have steps between themselves and the prospective internal base region, are left to form island regions. A sidewall insulating film is formed which covers at least a sidewall on the prospective collector region side among sidewalls of the external base region and sidewalls at the steps of the prospective internal base region adjoining the sidewalls of the external base region. The emitter region and collector

US-PAT-NO: 5399894

DOCUMENT-IDENTIFIER: US 5399894 A

TITLE: Semiconductor device having bipolar transistor and MOS transistor

--------- KWIC ---------

Next, as shown in FIG. 5C, a mixed crystal of silicon and germanium is formed and then a heat treatment (at 600.degree. to 900.degree. C.) is effected in order to crystallize the silicon. As a result, an internal base region (mixed crystal of silicon and germanium) 95a containing a P.sup.- -type impurity and an external base region 95b containing a P.sup.+ -type impurity and having an impurity concentration higher than the internal base region 95a are formed in the amorphous silicon layer 93. Further, arsenic is ion-implanted into the surface area of the amorphous silicon layer 94 at a high impurity concentration to form an N.sup.+ -type region. Next, the amorphous silicon layer 94 is patterned to form an emitter region. After this, an SiGe layer formed of the internal base region 95a and the external base region 95b is selectively etched to lie over the field oxide film 85 to form a base region. Next, an inter-level insulation film 96 is deposited on the entire surface by use of the CVD method, and then a heat treatment is effected at 1000.degree. C. for approx. 10 seconds. Contact holes reaching the base region and the like are

US-PAT-NO: 5336909

DOCUMENT-IDENTIFIER: US 5336909 A

TITLE: Bipolar transistor with an improved collector structure

--------- KWIC ---------

In the bipolar transistor of the present invention, it is effective that a layer of the second conductivity type having a concentration lower than the internal base region is formed in the external base region to be in contact with the third collector layer and to be separated from the first collector layer.

More specifically, since the layer of the second conductivity type having a concentration lower than that of the internal base region is formed in the external base region to be in contact with the third collector layer and to be separated from the first collector layer, the collector junction capacitance can be further minimized.

A p-type AlGaAs base layer 107 is formed on the collector layer. The

FIG. 1 (PRIOR ART)

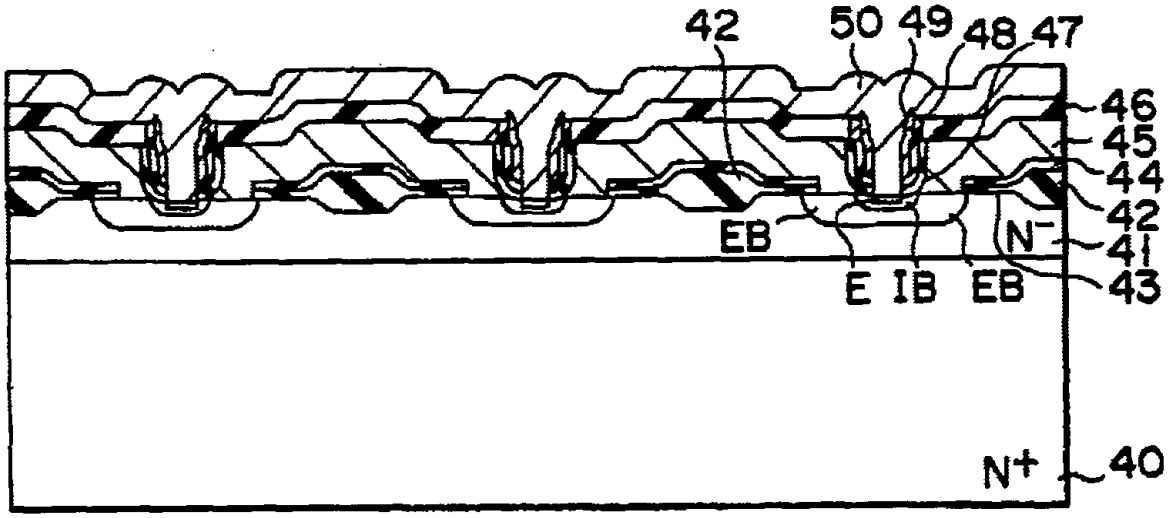


FIG. 2 (PRIOR ART)